Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **OUT 1**
2. **IN 1-**
3. **IN 1+**
4. **VCC-**
5. **IN 2+**
6. **IN 2-**
7. **OUT 2**
8. **VCC+**

**.084”**

**5 4 3**

**7 8 1**

**6**

**2**

**.065”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: Vcc-**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .065” X .084” DATE: 4/27/23**

**MFG: TEXAS INSTRUMENTS THICKNESS .012” P/N: TL062**

**DG 10.1.2**

#### Rev B, 7/19/02